WHAT IS CLAIMED IS:

1. A processor comprising:
a plurality of functional units; and
a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers.

2. A processor according to Claim 1 wherein:
the processor is a Very Long Instruction Word (VLIW) processor.

3. A processor according to Claim 1 wherein:
the local registers and global registers are addressed using register addresses in an address space that is defined for a register file segment/ functional unit pair.

4. A processor according to Claim 1 wherein:
the register file is a multi-ported register file.

5. A processor according to Claim 1 wherein:
the local registers in a register file segment are addressed using register addresses in a local register range outside the global register range that are assigned within a single register file segment/ functional unit pair.

6. A processor according to Claim 1 wherein:
register addresses in the local register range are the same for the plurality of register file segment/ functional unit pairs and address registers locally within a register file segment/ functional unit pair.

7. A processor according to Claim 1 wherein:
the register file includes N physical registers and is duplicated into M register file segments, the register file segments having a reduced number of read and/or write ports in comparison to a nonduplicated register file, but each having the same number of physical registers.

8. A processor according to Claim 7 wherein:
the register file segments are partitioned into N_G global and N_L local register files where N_G plus N_L is equal to N, the register file operating equivalently to a register file having $N_G + (M * N_L)$ total registers available for the M functional units, the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits B that are used to address $N = 2^B$ registers, the local registers for ones of the M register file segments are addressed using the same B-bit values.

9. A processor according to Claim 6 wherein:
partitioning of the register file is programmable so that the number N_G of global registers and number N_L of local registers is selectable and variable.

10. A processor according to Claim 1 wherein the register file is a storage array structure having R read ports and W write ports comprising:
a plurality of storage array storages;
the storage array storages having a reduced number of read ports so that the total number of read ports for the plurality of storage array storages is R read ports; and
the storage array storages having W write ports.

11. A processor according to Claim 10 wherein:
the storage array structure is a sixteen port structure with twelve read ports and five write ports; and
the plurality of storage array storages includes four storage array storages each having three read ports and five write ports.

12. A processor according to Claim 10 wherein:
the storage array structure is a sixteen port structure with twelve read ports and four write ports; and
the plurality of storage array storages includes four storage array storages each having three read ports and four write ports.

13. A processor according to Claim 10 wherein:
the writes are fully broadcast so that all of the storage array storages are held coherent.

14. A processor according to Claim 10 wherein:
storage array storages include storage cells having a plurality of word lines and a plurality of bit lines, the word lines being formed in one metal interconnect layer, the bits lines being formed in a second metal interconnect layer.

15. A processor comprising:
a decoder for decoding a very long instruction word including a plurality of subinstructions, the subinstructions being allocated into positions of the instruction word;
a register file coupled to the decoder and divided into a plurality of register file segments; and
a plurality of functional units, ones of the plurality of functional units being coupled to an associated with respective ones of the register file segments, ones of the plurality of subinstructions being executable

upon respective ones of the plurality of functional units, operating upon operands accessible to the register file segment associated with the functional unit of the plurality of functional units, the register file segments including a plurality of registers that are partitioned into global registers and local registers, the global registers being accessible by the plurality of functional units, the local registers in one of the register file segments being accessible by the functional unit associated with the register file segment.

16. A processor according to Claim 15 wherein:
the local registers and global registers are addressed using register addresses in an address space that is defined for a register file segment/ functional unit pair.

17. A processor according to Claim 15 wherein:
the register file is a multi-ported register file.

18. A processor according to Claim 15 wherein:
the local registers in a register file segment are addressed using register addresses in a local register range outside the global register range that are assigned within a single register file segment/ functional unit pair.

19. A processor according to Claim 15 wherein:
register addresses in the local register range are the same for the plurality of register file segment/ functional unit pairs and address registers locally within a register file segment/ functional unit pair.

20. A processor according to Claim 15 wherein:
the register file includes N physical registers and is duplicated into M register file segments, the register file segments having a reduced number of read and/or write ports in comparison to a nonduplicated register file, but each having the same number of physical registers.

21. A processor according to Claim 20 wherein:
the register file segments are partitioned into N_G global and N_L local register files where N_G plus N_L is equal to N, the register file operating equivalently to a register file having $N_G + (M * N_L)$ total registers available for the M functional units, the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits B that are used to address $N = 2^B$ registers, the local registers for ones of the M register file segments are addressed using the same B-bit values.

22. A processor according to Claim 20 wherein:
partitioning of the register file is programmable so that the number N_G of global registers and number N_L of local registers is selectable and variable.

23. A method of operating a processor comprising:
operating a plurality of functional units; and
dividing a register file into a plurality of register file segments;
coupling and associating ones of the plurality of register file segments with ones of the plurality of functional units;
partitioning the register file segments into global registers and local registers;
accessing the global registers by the plurality of functional units;
accessing the local registers by the functional unit associated with the register file segment containing the local registers.

24. A method according to Claim 23 further comprising:
addressing the local registers and global registers using register addresses in an address space that is defined for a register file segment/ functional unit pair.

25. A method according to Claim 23 further comprising:
addressing the local registers in a register file segment using register addresses in a local register range outside the global register range that are assigned within a single register file segment/ functional unit pair.

26. A method according to Claim 23 further comprising:
addressing the local register range the same for the plurality of register file segment/ functional unit pairs and address registers locally within a register file segment/ functional unit pair.

27. A method according to Claim 23 further comprising:
including N physical registers in the register file;
duplicated the physical registers into M register file segments, the register file segments having a reduced number of read and/or write ports in comparison to a nonduplicated register file, but each having the same number of physical registers.

28. A method according to Claim 27 further comprising:
partitioning the register file segments into N_G global and N_L local register files where N_G plus N_L is equal to N;
operating the register file equivalently to a register file having $N_G + (M * N_L)$ total registers available for the M functional units, the number of address bits for addressing the $N_G + (M * N_L)$ total registers being equal to the number of bits B that are used to address $N = 2^B$ registers; and
addressing the local registers for ones of the M register file segments using the same B-bit values.

29. A method according to Claim 27 further comprising:
programmably partitioning the register file so that the number N_G of global registers and number N_L of local registers is selectable and variable.